REMARKS

Overview of the Office Action

The Abstract has been objected to as including improper language and having an improper format.

Claims 1-8 and 12-15 have been rejected under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 6,100,104 ("Haerle") in view of U.S. Patent No. 5,693,962 ("Shi").

Claims 9-11 have been rejected under 35 U.S.C. §103(a) as unpatentable over Haerle in view of Shi, and further in view of U.S. Patent No. 6,110,177 ("Braun").

Status of the claims

Claim 1 has been amended

Claims 1-15 remain pending

Objection to the Abstract

The Abstract has been objected to as including improper language and being longer than 150 words. The Abstract has been amended to include only proper language and so that it is no longer than 150 words in length. Applicant submits that this objection has been overcome.

Rejection of claims 1-8 and 12-15 under 35 U.S.C. §103(a)

The Office Action states that the combination of Haerle and Shi teaches all of Applicant's recited elements. Applicant disagrees.

Independent claim 1 has now been amended to clarify its recitation of a method for the production of a plurality of optoelectronic semiconductor chips each having a plurality of structural elements, with each structural element comprising a semiconductor layer sequence,

that includes the steps of "forming on the growth surface a mask material layer with a multiplicity of windows, most of which have an average lateral extent of less than or equal to 1 μm, wherein a mask material is chosen so that a semiconductor material of the semiconductor layer that is to be grown in a later method step essentially cannot grow on said mask material or can grow in a substantially worse manner in comparison with the growth surface". Support for these claim amendments can for example be found in paragraphs [0012] and [0038] of Applicants' published specification.

Haerle and Shi, whether taken alone or in combination, fail to teach or suggest the steps of "forming on the growth surface a mask material layer, with a multiplicity of windows, most of which have an average lateral extent of less than or equal to 1 μm", "essentially simultaneously growing semiconductor layers to form the structural elements on regions of the growth surface that lie within the windows", and "singulating the chip composite base with applied material to form semiconductor chips each having a plurality of the structural elements", as recited in Applicant's amended claim 1.

Applicant's recited invention is directed to a method for the production of a plurality of optoelectronic semiconductor chips, each having a plurality of structural elements 12 and each structural element comprising a semiconductor layer sequence. Applicant's recited method includes, with illustrative reference to the depicted structure, providing a chip composite base 5 having a substrate 4, a semiconductor layer or layer sequence 6, and a growth surface 3, and forming on the growth surface 3 a mask material 11 with a multiplicity of windows 2, most of which have an average lateral extent of less than or equal to 1 μm. The mask material 1 is chosen so that a semiconductor material of the semiconductor layer that is to be grown in a later method step essentially cannot grow on the mask material or can only grow on the mask material

in a substantially worse manner as compared with the growth surface 3. Applicant's recited method further includes essentially simultaneously growing semiconductor layers 8 to form the structural elements 12 on regions of the growth surface 3 that lie within the windows 2, and singulating the chip composite base 5 with applied material to form a plurality of semiconductor chips that each have a plurality of structural elements where each of the structural elements includes a semiconductor layer sequence (see Fig. 2 of Applicant's specification).

The semiconductor layer sequence 6 arranged on the substrate 4 can have an active zone that emits electromagnetic radiation when a voltage is applied (see paragraph [0051] of Applicant's specification).

As described in Applicant's specification, "lateral extent is the length of a window projected onto a straight line, the straight line running in a principal extending plane of the mask material layer. The average lateral extent is accordingly the extent of a window averaged over all directions" (see paragraph [0012] and Fig. 1D of Applicant's specification). In other words, the average lateral extent is the "lateral extent" of a window 2 averaged over all directions that lie within the principal extending plane of the mask material layer 11 (i.e., all lateral directions of the window 2 in Fig. 1D).

Haerle discloses a method for fabricating a plurality of LED semiconductor bodies. According to the method of Haerle, the plurality of LEDs are produced by first depositing a mask layer on a main surface of a substrate wafer. A plurality of windows are then formed in the mask layer of Haerle such that the wafer surface is laid bare in the windows. A semiconductor layer sequence that functionally defines the semiconductor bodies is then deposited onto the main surface in the windows of Haerle. Finally, the wafer of Haerle is divided and severed into individual LEDs (see Figs. 5 and 6 and the Abstract of Haerle).

The Examiner cites Fig. 4 of Haerle as allegedly teaching essentially simultaneously growing semiconductor layers to form the structural elements on regions of the growth surface that lie within the windows.

According to Haerle, the semiconductor layers, which are deposited on the substrate surface through the mask windows, functionally form the LEDs (see col. 7, lines 1-5 of Haerle). Nothing in Haerle teaches or suggests that the deposited semiconductor layers form structural elements of the resulting semiconductor bodies, or that each of the resulting chips include a plurality of structural elements each comprising a semiconductor layer sequence, as expressly recited in Applicant's claim 1.

The Examiner also cites col. 7, lines 33-36 and Figs. 5-6 of Haerle as allegedly teaching singulating the chip composite base with applied material to form semiconductor chips each having a plurality of structural elements.

The cited passages and figures of Haerle in fact teach that once the chip is singulated, each resulting device comprises a semiconductor sequence forming a single LED without any structural elements. This teaching is in stark contrast to Applicant's recited method in which chip singulation of the composite base with applied material results in the formation of a plurality of semiconductor chips, each of which includes a plurality of structural elements each comprising a semiconductor layer sequence.

Furthermore, as is well known to those skilled in the art, the lateral dimensions of optoelectronic semiconductor chips are typically on the order of several hundred μm, with smaller chips having a length of approximately 250 μm, and larger chips having a length of approximately 1000 μm. There is nothing in Haerle that states or suggests that its optoelectronic chips are anything other than standard-sized. Therefore, it follows that the semiconductor layer

sequence of each chip taught by Haerle must be in the general range of about 250 to 1000 μm in its lateral dimensions. Consequently, the semiconductor layer sequence taught by Haerle is wholly unrelated and non-analogous to the plurality of structural elements recited in Applicant's claims, which result in chips on the order of 1 μm or less in lateral dimension. The lateral dimensions of Applicant's recited structural elements are thus more than two magnitudes smaller than the lateral dimensions of the semiconductor layer sequence taught by Haerle, since Applicant's structural elements are produced by selective growth within a very small window having an average lateral extent of less than or equal to 1 μm, as discussed above.

In response to Applicant's previous arguments, the Examiner states that according to page 8, lines 15-28 of Applicant's specification "the semiconductor layer sequence forms the structural element".

Applicant submits that the Examiner has misinterpreted Applicant's specification. The meaning of the sentence cited by the Examiner is that each structural element is formed by growing a semiconductor layer sequence in the window of the mask layer (i.e., the material of the structural element is the combination of both the semiconductor layer sequence and the shape of the structural element as defined by the mask window).

Even if one skilled in the art were to interpret the semiconductor layer sequence of Haerle as being a structural element, Haerle merely discloses chips each having only one structural element, i.e., the single semiconductor layer sequence. In contrast to Haerle, on the other hand, Applicant's recited invention requires that each chip have a plurality of structural elements with each of these structural elements comprising a semiconductor layer sequence.

Haerle, therefore, fails to teach or suggest "essentially simultaneously growing semiconductor layers to form the structural elements on regions of the growth surface that lie

within the windows", and "singulating the chip composite base with applied material to form semiconductor chips each having a plurality of structural elements", where each of the structural elements comprises a semiconductor layer sequence, as recited in Applicant's amended independent claim 1.

The Examiner concedes that Haerle fails to teach or suggest forming on the growth surface a mask material layer with a multiplicity of windows, most of which have an average extent of less than or equal to 1 μm. However, the Examiner cites col. 4, lines 15-27, and col. 5, line 66 to col. 6, line 8 of Shi as allegedly teaching a multiplicity of windows, most of which have an average extent of less than or equal to 1 μm, and interprets the phrase "average extent" as including the depth of the windows.

Shi discloses an organic full color light emitting diode array that includes a plurality of spaced apart, light transmissive electrodes formed on a substrate, a plurality of cavities defined on top of the electrodes, and three electroluminescent media designed to emit three different hues deposited in the cavities. A plurality of spaced metallic electrodes are arranged orthogonal to the light transmissive electrodes of Shi and are formed to seal each of the cavities, thereby sealing the electroluminescent media in the cavities. A light transmissive anodic electrode is disposed at the bottom of each cavity of Shi, and an ambient stable cathodic metallic electrode is disposed on the top of each cavity (see Abstract of Shi).

As discussed above, Applicant's claim 1 has been amended to now recite an "average lateral extent", thus clarifying that it refers to the lateral extent of a window 2 averaged over all directions that lie within the principal extending plane of the mask material layer 11. Thus, the recited phrase "average lateral extent" cannot refer to a vertical extent or depth of the window 2. With Applicant's smaller windows in the mask material layer, it is thereby possible to produce

smaller structural elements in a larger area density (see paragraph [0013] of Applicant's specification). The depth of the window 2 quite obviously has no significance when the provision of a large area density of structural elements is to be achieved.

In contrast to Applicant's now clarified recited "average lateral extent", the cited passages of Shi refer to the depth of cavity structure 112, not to an average of its lateral dimensions. Shi merely discloses that the thickness of the dielectric medium 103 determines the depth of the cavity structure and can be less than 1 µm (see col. 4, lines 25 to 27 of Shi), the lateral extent of the cavity structure being significantly larger (see col. 5, line 66 to col. 6, line 8 of Shi). The cited passages of Shi also disclose a pixel pitch, which is simply the distance between adjacent pixels and not the size of each pixel, and thus does not relate to, teach, or suggest Applicant's recited average lateral extent of less than or equal to 1 µm.

Further, there is no reason that one skilled in the art would look to reduce the width of the mask windows of Haerle to a size of 1 µm or less, absent Applicant's teachings, because such a size window would result in individual chips having a dimension of only 1 µm x 1 µm or less. Typical LED chips have a size of about 0.5 mm x 0.5 mm or more (i.e., the area of a standard LED chip is upwards of about 500 x 500 = 25000 times greater than a chip with a dimension of only 1 µm x 1 µm or less). An LED chip with a size of only 1 µm x 1 µm would have an extremely low, barely perceivable illumination brightness, and the person of skill would not therefore have a reason to create such an LED chip. Shi, indeed, discloses or suggests no reason that one skilled in the art would wish to reduce the average lateral dimensions of the cavity to 1 µm or less.

Shi, therefore, fails to teach or suggest "forming on the growth surface, a mask material layer with a multiplicity of windows, most of which have an average lateral extent of less than or

equal to 1 μm", as expressly recited in Applicant's amended claim 1. Further, Shi also fails to teach or suggest "essentially simultaneously growing semiconductor layers to form the structural elements on regions of the growth surface that lie within the windows", and "singulating the chip composite base with applied material to form semiconductor chips each having a plurality of the structural elements", all as recited in Applicant's amended claim 1.

Consequently, Haerle and Shi, whether taken alone or in combination, fail to teach or suggest each of the steps recited in Applicant's amended claim 1.

Claim 14 recites limitations corresponding to those of claim 1 and is, therefore, deemed to be patentably distinct over Haerle and Shi for at least those reasons discussed above with respect to independent claim 1.

In view of the foregoing, Applicant submits that Haerle and Shi, whether taken alone or in combination, fail to teach or suggest the subject matter recited in independent claims 1 and 14. Accordingly, claims 1 and 14 are patentable over Haerle and Shi under 35 U.S.C. §103(a).

Dependent claims

Claims 2-8, 12-13, and 15, which depend from independent claim 1, incorporate all of the limitations of independent claim 1 and are, therefore, deemed to be patentably distinct over Haerle and Shi for at least those reasons discussed above with respect to independent claim 1.

Rejection of claims 9-11 under 35 U.S.C. §103(a)

The Office Action states that the combination of Haerle, Shi and Braun teaches all of Applicant's recited steps in these claims.

Haerle and Shi have been previously discussed and do not teach or suggest the subject matter recited in Applicants' independent claim 1.

Because Haerle and Shi fail to teach or suggest the subject matter recited in Applicant's independent claim 1, and because Braun does not teach or suggest any of the method steps of independent claim 1 that Haerle and Shi are missing, the addition of Braun to the reference combination fails to remedy the above-described deficiencies of Haerle and Shi.

Claims 9-11, which depend from independent claim 1, incorporate all of the limitations of independent claim 1 and are, therefore, deemed to be patentably distinct over Haerle, Shi and Braun for at least those reasons discussed above with respect to independent claim 1.

Conclusion

In view of the foregoing, reconsideration and withdrawal of all rejections, and allowance of all pending claims, is respectfully solicited.

Should the Examiner have any comments, questions, suggestions, or objections, the Examiner is requested to telephone the undersigned to facilitate an early resolution of any outstanding issues.

Respectfully submitted,
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